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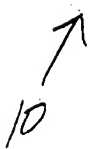


Fig. 1

MULTI-LAYER INTEGRATED SEMICONDUCTOR STRUCTURE

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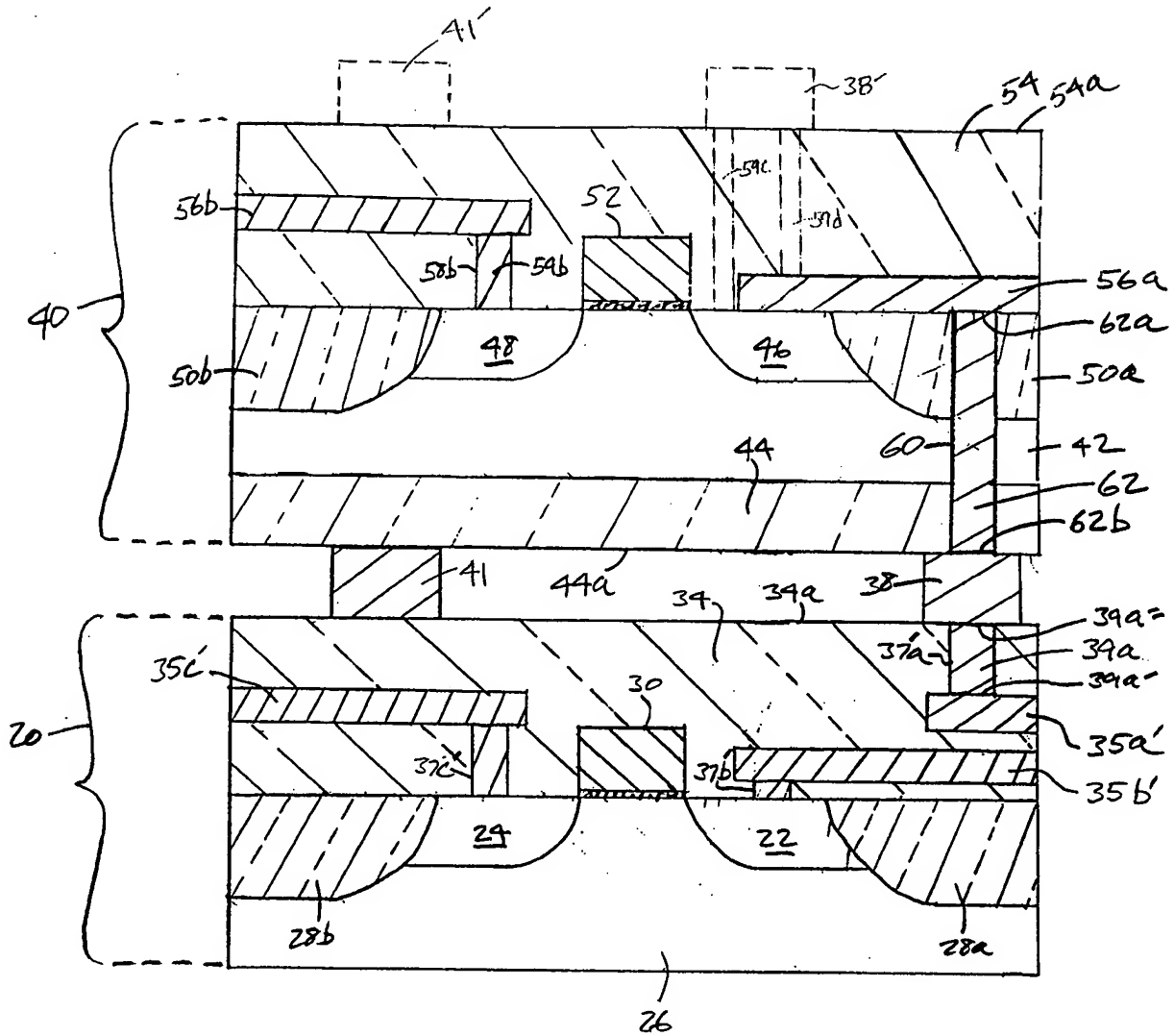


Fig. 2.



Fig. 3

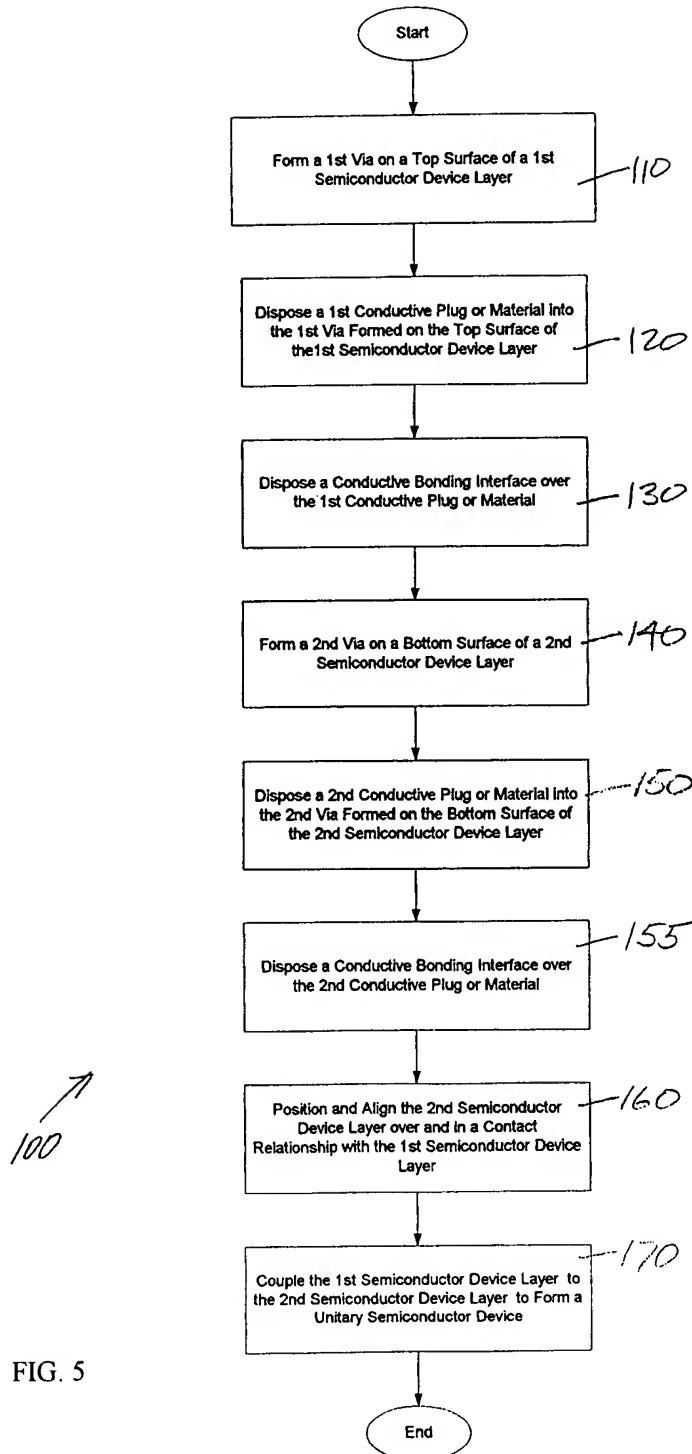
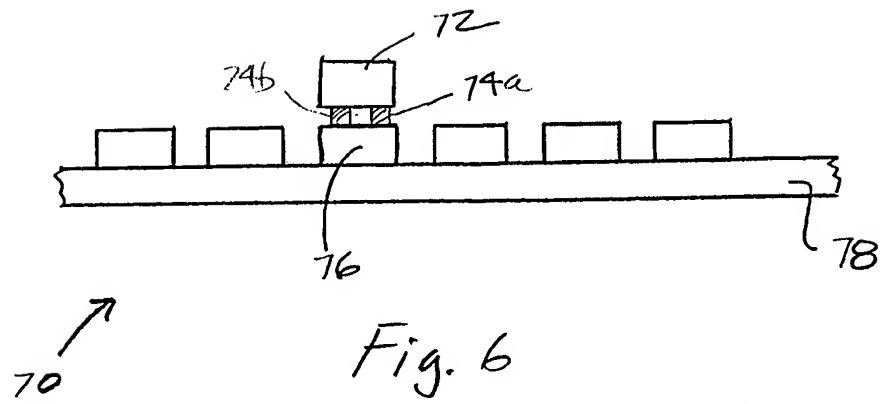


FIG. 5



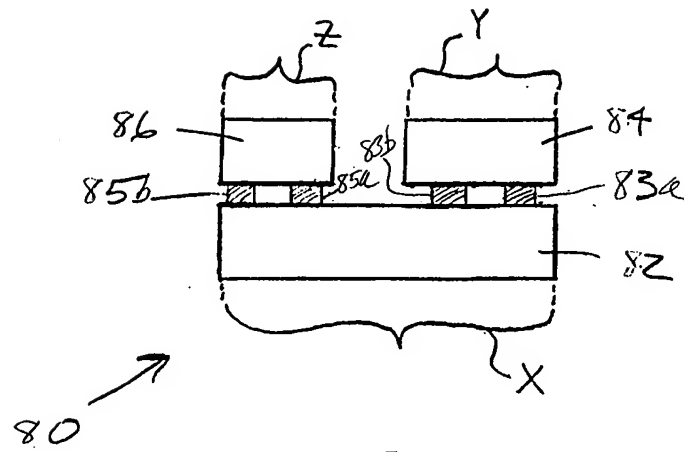


Fig. 7